UNITED STATES PATENT AND TRADEMARK OFFICE

A

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,797	06/26/2003	Tetsuroo Honmura	501.42810X00	3466

20457 7590 10/25/2005

ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-3873

EXAMINER	
NGUYEN, TANH Q	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 10/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/603,797	HONMURA, TETSUROO	
	Examiner	Art Unit	
	Tanh Q. Nguyen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 2-4 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 2-4 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 2-4 are objected to because of the following informalities: "The" in line 1 of claim 2 should be replaced with "A".

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 2 is rejected under 35 U.S.C. 102(b) as anticipated by **Takeda (USP 6,292,851)**

Takeda teaches a semiconductor integrated circuit [6, FIG. 1] comprising:

a nonvolatile memory [30, FIG. 2] to store address information [address conversion table: col. 5, lines 22-24] indicating a relationship between an address of a first memory space [MEMORY ADDRESS SPACE, FIG. 10] and an address of a second memory space [PHYSICAL ADDRESS SPACE, FIG. 10];

a plurality of functional modules [LSI ALARM A, LSI ALARM B, LSI ALARM C, FIG. 10] each having an address in the second memory space [FIG. 10; col. 6, lines 52-60]; and

a bus control circuit [16, FIG. 2],

wherein the bus control circuit receives a first address in the first memory space

and translates the first address into a second address in the second memory space using the address information [col. 5, line 62-col. 6, line 5] and access is made to a functional module having the second address among the plurality of functional modules [col. 6, line 5-9];

a bus [IN, OUT, 36, 38, 40 - FIG. 2]; and

a switching circuit to control a connection between the plurality of functional modules and the bus [a control program entering a loop to read status registers of the functional modules [col. 5, lines 7-10], when the control program reads a specific status register of a specific functional module [one of functional modules 17], the specific functional module is activated to send register data on the data bus [col. 5, lines 11-14] - hence a connection of the specific functional module and the bus],

wherein the nonvolatile memory stores connect/disconnect information for the plurality of functional modules [the nonvolatile memory storing the control program [col. 5, lines 4-5] and control program entering a loop to read status registers of the functional modules [col. 5, lines 7-10] - hence the control program storing connect/disconnect information for the plurality of functional modules (i.e. information as to which of the functional modules are activated and deactivated during the execution of the loop), and

the switching circuit selects a functional module to be connected with the bus according to the connect/disconnect information [the control program selects a specific functional module and reads data from that functional module [col. 5, lines 11-14]].

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Takeda**.

Takeda teaches the address information being changed in the nonvolatile memory (hence stored in the nonvolatile memory) when the physical addresses of the functional modules are changed, e.g. when engineering changes are made to the semiconductor integrated circuit [col. 6, line 67-col. 7, line 2; col. 6, lines 60-62], and the nonvolatile memory being modifiable by on-board reprogramming [col. 7, lines 32-34].

Since a probing test is normally conducted in association with an engineering change, and since the nonvolatile memory is modifiable by on-board reprogramming, it would have been obvious to one of ordinary skill in the art at the time the invention was made to store the address information in the nonvolatile memory (by on-board reprogramming) when a probing test (associated with an engineering change) is conducted is on the semiconductor integrated circuit in order to reflect a proper relationship between the address of the first memory space and the address of the second memory space, and in order to allow Takeda's system to function properly.

Furthermore, since the physical addresses of the functional modules can be

changed [col. 6, lines 60-62] and the control program uses the addresses of the functional modules to read registers of the functional modules [col. 5, lines 11-14; col. 5, lines 18-20], a change in the physical address of the functional modules when a probing test (associated with an engineering change) is conducted is on the semiconductor integrated circuit would also result in the connect/disconnect information being changed - hence the connect/disconnect information being stored in the nonvolatile memory.

6. Claims 2-4 are alternatively rejected under 35 U.S.C. 103(a) as being unpatentable over **Takeda** in view of **Uffenbeck (Microcomputers and Microprocessors: The 8080, 8085, and Z-80 Programming, Interfacing, and Troubleshooting pp 148-160)**.

Uffenbeck teaches a data bus with many transmitters [page 155, FIG. 4.21; page 155, Type 3 Bus, lines 1-7] between a plurality of functional modules [Input devices, FIG. 4.21] and the data bus, each transmitter being a tri-state gate that is enabled to gate data onto a data bus line [FIG. 4.18 (a), (b) - page 152], and that is disabled to allow the data bus line to be controlled by another transmitter [FIG. 4.18 (c) page 152] to allow a plurality of functional modules to access the same bus and avoid interference [page 153, lines 1-3] - hence teaches a switching circuit to control a connection between the plurality of functional modules and the bus to allow a plurality of functional modules to access the same bus and avoid interference [page 153, lines 1-3].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a Type 3 bus with a switching circuit, as is taught by

Uffenbeck, as the data bus in Takeda - in order to allow the plurality of functional modules of Takeda to access the same data bus and avoid interference.

7. Claims 2-4 are also alternatively rejected under 35 U.S.C. 103(a) as being unpatentable over **Takeda** in view of **Cupps et al. (US 2003/0226044 A1)**.

Cupps teaches functional modules that are not necessary for the tasks at hand to be disabled (i.e. disconnected from a bus) to save power [[0053]] - hence teaches a switching circuit to control a connection between the plurality of functional modules and the bus to save power.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a switching circuit, as is taught by Cupps, in Takeda's integrated circuit to disconnect functional modules that are not necessary for the tasks at hand to be disconnected in order to save power.

Double Patenting

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

9. Claims 2-4 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over **claims 7-10 of Honmura (USP 6,845,496)** in view of **Takeda**.

10. As per claim 2, claims 7-9 of **Honmura** claim a semiconductor integrated circuit comprising:

a memory [claim 8, line 2];

a plurality of functional modules [first and second circuit modules - claim 7, lines 5, 8];

a bus [claim 7, line 3]; and

a switching circuit [first and second switching elements - claim 7, lines 11,15] to control a connection between the plurality of functional modules and the bus [claim 7, lines 11-18],

wherein the memory stores connect/disconnect information for the plurality of functional modules [first and second control signals - claims 8-9], and the switching circuit selects a functional module to be connected with the bus according to the connect/disconnect information [claim 7, lines 11-18; claims 8-9].

Claims 7-9 of Honmura do not claim the memory being nonvolatile. Since it was known in the art at the time the invention was made to use nonvolatile memory to retain information when the power is removed from a system, it would have been obvious to

one of ordinary skill in the art at the time the invention was made to store the connect/disconnect information in a nonvolatile memory in order to retain the connect/disconnect information when power to the system is removed.

Claims 7-9 of Honmura do not claim the nonvolatile memory storing address information indicating a relationship between an address of a first memory space and an address of a second memory space; each of the plurality of functional modules having an address in the second memory space; and a bus control circuit, wherein the bus control circuit receives a first address in the first memory space and translates the first address into a second address in the second memory space using the address information and access is made to a functional module having the second address among the plurality of functional modules.

Takeda teaches a nonvolatile memory [30, FIG. 2] storing address information [address conversion table: col. 5, lines 22-24] indicating a relationship between an address of a first memory space [MEMORY ADDRESS SPACE, FIG. 10] and an address of a second memory space [PHYSICAL ADDRESS SPACE, FIG. 10]; a plurality of functional modules [LSI ALARM A, LSI ALARM B, LSI ALARM C, FIG. 10] each having an address in the second memory space [FIG. 10; col. 6, lines 52-60]; and a bus control circuit [16, FIG. 2], wherein the bus control circuit receives a first address in the first memory space and translates the first address into a second address in the second memory space using the address information [col. 5, line 62-col. 6, line 5] and access is made to a functional module having the second address among the plurality of functional modules [col. 6, line 5-9] - to allow for modification of register addresses of

functional modules in a supervised module without modifying a control program in a supervisory module [col. 7, lines 15-18].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Takeda's aforementioned teachings - in order to allow for modification of register addresses of functional modules in a supervised module without modifying a control program in a supervisory module.

11. As per claim 3, Takeda teaches the address information being changed in the nonvolatile memory (hence stored in the nonvolatile memory) when the physical addresses of the functional modules are changed, e.g. when engineering changes are made to the semiconductor integrated circuit [col. 6, line 67-col. 7, line 2; col. 6, lines 60-62], and the nonvolatile memory being modifiable by on-board reprogramming [col. 7, lines 32-34].

Since a probing test is normally conducted in association with an engineering change, and since the nonvolatile memory is modifiable by on-board reprogramming, it would have been obvious to one of ordinary skill in the art at the time the invention was made to store the address information in the nonvolatile memory (by on-board reprogramming) when a probing test (associated with an engineering change) is conducted is on the semiconductor integrated circuit in order to reflect a proper relationship between the address of the first memory space and the address of the second memory space, and in order to allow Takeda's system to function properly.

12. As per claim 4, claim 10 of Honmura claims programmed data being entered

from the outside - hence the connect/disconnect information being stored in the nonvolatile memory when a probing test is conducted on the semiconductor integrated circuit.

Response to Arguments

13. Applicant's arguments with respect to claims 2-4 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tanh Quang Nguyen whose telephone number is (571) 272-4154 and whose e-mail address is tanh.nguyen36@uspto.gov. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh, can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300 for After Final, Official, and Customer Services, or (571) 273-4154 for Draft to the Examiner (please label "PROPOSED" or "DRAFT").

Effective May 1, 2003 are new mailing address is:

Mail Stop ____
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Effective December 1, 2003, hand-carried patent application related incoming correspondences will be to a centralized location.

U.S. Patent and Trademark Office
2011 South Clark Place
Customer Window
Crystal Plaza Two, Lobby, Room 1B03
Arlington, VA 22202

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197.

10/20/2005

TQN
October 20, 2005